REMARKS

A. Information Disclosure Statement

In paragraph 2 (on page 2) of the office action of October 6, 2005, the Examiner objects that a list of references in a specification is not a proper information disclosure statement. Applicants assure the Examiner that the incorporation by reference of other patents or applications in the specification was not intended to substitute for an information disclosure statement. The references to be cited in an information disclosure statement were so cited in the IDS filed on March 3, 2004. If any additional references are to be cited, of course supplemental IDSs will be filed.

B. Specification Objections

The Examiner objected to paragraph [0001] of the specification, requiring that the Applicant supply the application serial number of the application by Cleeves et al., which was filed the same day as the present application, and thus unavailable at the time of filing. Applicant has amended the specification as required, providing this application serial number and deleting the attorney docket number.

This specification amendment does not constitute new matter.

C. Drawing Objections

The Examiner objected to the drawings, believing them not to show the fourth pitch substantially less than or substantially one half of the first pitch as recited in claims 28, 29, 43, 69, and 85.

Applicants respectfully direct the Examiner's attention to Fig. 5, which shows memory lines having a fourth pitch P_M which is substantially less than, or one-half of, the first pitch P_V of the vias. Via pitch P_V is also shown in Fig. 6, which shows the vias in a

cross-sectional view. Paragraphs [0038] and [0039] of the specification describe Figures 5 and 6.

Applicants wish to be fully cooperative with the Examiner's requirements, but, as the first and fourth pitch of claims 28, 29, 43, 69, and 85 in fact are shown in the figures, Applicants have made no drawing amendments. Applicants are happy to discuss any clarification the Examiner may wish to suggest.

D. Status of the Claims

Claims 1-94 are pending in the application. Claims 16-26, 44-54, 70-72, and 75-80 are withdrawn from consideration. Claims 1, 15, 30, and 56 were rejected under 35 USC 112, second paragraph. Claims 1-6, 30-34, 56-60, 74, 81-84, and 94 were rejected under 35 USC 102(b) as being anticipated by Iwasaki, US Patent No. 6,034,436. Claims 1, 2, 4-7, 15, 28-33, 35, 43, 56-59, 69, 74, 81-83, 85, 86, and 94 were rejected under 35 USC 102(b) as being anticipated by Amanuma, US Publication No. 2001/0038115.

Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93 were rejected under 35 USC 103(a) as being unpatentable over Iwasaki.

E. 35 USC 112 Rejections: Claims 1, 15, 30, and 56

Claims 1, 15, 30, and 56 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Examiner correctly pointed out that the term "the substrate" in claim 1 lacked antecedent basis. Claim 1 has been cancelled, and its limitations included in claim 6, where the error has been corrected.

The term "the memory lines" in claim 15 similarly lacked antecedent basis. This claim has been amended to depend from claim 6, which provides the required antecedent.

The Examiner also correctly identified lack of antecedent basis for the term "the substrate" in claim 30. Claim 30 has been cancelled, and its limitations included in claim 33, where the error has been corrected.

A third instance of the same error was also identified by the Examiner in claim 56. Claim 56 has been cancelled, and its limitations included in claim 59, where the error has been corrected.

Applicants appreciate the Examiner's identification of these errors.

F. 35 USC 102(b) Rejections: Claims 1-6, 30-34, 56-60, 74, 81-84, and 94

Claims 1-6, 30-34, 56-60, 74, 81-84, and 94 were rejected under 35 USC 102(b) as being anticipated by Iwasaki.

Claims 1-5 have been cancelled.

Claim 6 has been amended to recite a structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising: a first plurality of vias, each having a top end and a bottom end; a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping; a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via; and a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height, wherein both routing levels are formed above a substrate, wherein the first and second vias are evenly spaced and have a common first pitch, and further comprising a third routing level, the

third routing level above the first and second vias connected at the top end of each first and second via, vertically opposite the first and second routing levels, wherein the third routing level comprises memory lines in a memory array.

In rejecting claim 6, the Examiner says:

> ... the third routing levels are memory lines. Iwasaki discloses an improved through hole structure and teaches that through hole/interconnect structures are used for memory arrays.

Applicants respectfully assert, however, that a teaching that the through-hole structures of Iwasaki are used in a memory array is not the same as a teaching that the third (upper) routing levels U1, U2, and U3 of Iwasaki are in fact *memory lines*, as recited in the claim. Memory lines are lines connecting directly to and addressing pluralities of memory cells in an array; examples of memory lines are shown in plan view in Fig. 5 of the present application. Such lines may be, for example, channel bodies arranged in a NAND series string. Alternatively, such memory lines may be conductors; two pluralities of such parallel conductors may be formed perpendicular to each other, one plurality above the other, with passive memory elements formed at their intersections.

Applicants can find no teaching in Iwasaki whether the connectors U1, U2, and U3 are memory lines, are continuous with memory lines, or are connected indirectly to memory lines. Structures U1, U2, and U3 are described only as "fourth layer interconnects" by Iwasaki, but no description of their relation to memory lines is provided. Thus claim 6 distinguishes over Iwasaki. Claims 7-15 depend from claim 6, and thus also distinguish over the reference.

Claims 30-32 have been cancelled. Claim 33 distinguishes over Iwasaki by the same rationale described for claim 6. Claim 34 depends from claim 33 and thus also distinguishes.

Claims 56-58 have been cancelled. Claim 59 distinguishes over Iwasaki by the same rationale described for claim 6. Claim 60 depends from claim 59 and thus also distinguishes.

Claims 74, 81 and 82 have been cancelled. Claim 83 distinguishes over Iwasaki for the same rationale provided for claim 6. Claim 84 depends from claim 83 and thus also distinguishes.

Claim 94 has been cancelled.

Applicants respectfully request reconsideration.

G. 35 USC 102(b) Rejections: Claims 1, 2, 4-7, 15, 28-33, 35, 43, 56-59, 69, 74, 81-83, 85, 86, and 94

Claims 1, 2, 4-7, 15, 28-33, 35, 43, 56-59, 69, 74, 81-83, 85, 86, and 94 were rejected under 35 USC 102(b) as being anticipated by Amanuma.

Claims 1, 2, 4, and 5 have been cancelled.

Claim 6 has been amended to recite a structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising: a first plurality of vias, ***each having a top end and a bottom end***; a second plurality of vias, ***each having a top end and a bottom end***, wherein the first and second pluralities of vias are vertically overlapping; a first routing level at a first height, said first level connected to the first plurality of vias ***at the bottom end*** of each first via; and a second routing level at a second height, said second level connected to the second plurality of vias ***at the bottom end*** of

each second via, wherein the first height is different from the second height, wherein both routing levels are formed above a substrate, wherein the first and second vias are evenly spaced and have a common first pitch, and further comprising a third routing level, the third routing level above the first and second vias connected ***at the top end*** of each first and second via, vertically opposite the first and second routing levels, wherein the third routing level comprises memory lines in a memory array.

As amended, in the claim the first and second routing levels are at the bottom end of the first and second vias, while the third routing level is at the top end of those vias.

If the location of contact 10 of Amanuma is considered to be the bottom end of via 12 on the right side in Fig. 2 of Amanuma, then the location 7 of via 12 on the left side of that figure cannot be considered its bottom end; its bottom end must be considered to be 10 as well. In fact, either via 12 is merely the segment between contacts 10 and 13, in which case both left and right vias 12 have contact 10 at their bottom ends; or via 12 is the entire vertical interconnect between contacts 4 and 18, in which case both left and right vias 12 have contact 4 at their bottom ends. In either case, the bottom ends of the left and right via 12 are at the same height, not at different heights as in the claim. As amended, claim 6 distinguishes over the vias of Amanuma.

Claims 14 and 15 depend from claim 6.

Claim 28 has been amended to recite a structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising: a first plurality of vias, ***each having a top end and a bottom end***; a second plurality of vias, ***each having a top end and a bottom end***, wherein the first and second pluralities of vias are vertically overlapping; a first routing level at a first height, said first level connected to the first

plurality of vias ***at the top end or at the bottom end*** of each first via; and a second routing level at a second height, said second level connected to the second plurality of vias ***at the top end or at the bottom end*** of each first via, wherein the first height is different from the second height, wherein both routing levels are formed above a substrate, wherein a) the first routing level and the second routing level are above the first and second vias or b) the first routing level and the second routing level are below the first and second vias, wherein the first and second vias are evenly spaced and have a common first pitch, and further comprising a third routing level, the third routing level above the first and second vias connected ***at the top end*** of each first and second via, or below the first and second vias connected ***at the bottom end*** of each first and second via, vertically opposite the first and second routing levels, wherein the third routing level has a fourth pitch substantially less than the first pitch. Claim 28 distinguishes over Amanuma by the same rationale described for claim 6.

Claim 29 depends from claim 28 and thus also distinguishes.

Claims 30-32 have been cancelled. Claim 33 distinguishes over Amanuma by the same rationale described for claim 6.

Claims 35 and 43 depend from claim 33 and thus also distinguish.

Claims 56-58 have been cancelled. Claim 59 distinguishes over Amanuma by the same rationale described for claim 6.

Claim 69 depends from claim 59 and thus also distinguishes.

Claims 74, 81, and 82 have been cancelled.

Claim 83 has been amended to recite a method for forming a via and routing structure for electrically connecting a multilevel array in an integrated circuit, the method

comprising: forming a first routing level; forming a second routing level above the first routing level; forming a first plurality of vias connected ***at bottom ends*** to the first routing level; forming a second plurality of vias connected ***at bottom ends*** to the second routing level, wherein the first and second pluralities of vias are vertically overlapping, wherein the multilevel array comprises a row of vias having a first pitch, the row of vias comprising the first plurality of vias and the second plurality of vias, vias of the first and second pluralities interspersed, further comprising forming a third routing level above the first and second routing levels, wherein said third routing level connects ***to top ends*** of the first plurality of vias or said third routing level connects ***to top ends*** of the second plurality of vias, wherein the third routing level comprises memory lines in a memory array.

As in claims 6, 33, and 59, claim 83 describes first and second routing levels at ***bottom ends*** of the first and second vias. Claim 83 thus distinguishes over the reference by the same rationale.

Claims 85 and 86 depend from claim 83 and thus also distinguish.

Claim 94 has been cancelled.

Applicants respectfully request reconsideration.

G. 35 USC 103(a) Rejections: Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93

Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93 were rejected under 35 USC 103(a) as being unpatentable over Iwasaki.

Claims 7-14 depend from claim 6, which distinguishes over the references for the reasons described in Section F of these remarks. Similarly, claims 35-42 depend from claim 33, which distinguishes over the references for the reasons described in Section F

of these remiuks. Claims 61-68 depend from claim 59, which distinguishes over the references for the reasons described in Section F of these remarks. Similarly, claims 86 93 depend from claim 83, which distinguishes over the references for the reasons described in Section F of these remarks.

In addition, claim 14 adds the limitation that the memory array is a monolithic three dimensional memory array. The Examiner finds that Iwasaki does not explicitly teach use of staggered vias of the claim in a monolithic three dimensional memory array:

> ... it is considered nonetheless obvious to one of ordinary skill in the art to employ the improved through-hole structure of Iwasaki to any known memory device structure or array.

Applicants will respectfully assert, however, that the simple fact that a structure, such as the interconnect structure of Fig. 7b of Iwasaki, is known, does not make its use desirable, or obvious, in every memory array. If this were the case, this interconnect structure would be widely used in memory arrays, but, as the Examiner will be aware, it is not. Many reasons, including complexity of interconnect fabrication and layout constraints, will lead those skilled in the art to choose other interconnect methods.

A monolithic three dimensional memory array, having multiple stacked device levels formed above a substrate, has very specific layout requirements. Several such memory arrays have been described, as in Johnson et al., US Patent No. 6,034,882; in Zhang, US Patent No. 5,835,396; in Cleeves, US Patent No. 6,664,639; and in Scheuerlein et al., US Publication No. 2004/0125629. None of these monolithic three dimensional memory arrays uses or suggests the use of the through-holes of Iwasaki, despite having the motivation suggested by the Examiner, "to reduce the occupied area for the interconnections." Absent some suggestion that such interconnects are

particularly advantageous in this context, Applicants maintain a *prima facie* case of obviousness has not been made.

The same rationale applies to the rejection of claims 27, 42, 55, 68, 73, and 90.

Claim 94 has been cancelled.

Applicants respectfully request reconsideration.

CONCLUSION

In view of the preceding Remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicants **respectfully request an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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